REMARKS/ARGUMENTS

After the foregoing amendment, claims 1-24 are currently pending in this application. Claim 12 has been amended to more clearly recite inventive subject matter. Support for the amendment is found at least in Fig. 2 and paragraph [0059]. No new matter has been introduced into the application by the amendment.

Claim Rejections - 35 USC § 112

Claims 1, 11, 12, 21, and 24 stand rejected under 35 USC § 112 second paragraph as being allegedly indefinite, because it is not clear to the Examiner what is meant by the abbreviation "SERDES." SERDES is a standard term in the art of data communications. Wikipedia defines it as "a pair of functional blocks commonly used in high speed communications. These blocks convert data between serial data and parallel interfaces in each direction." (http://en.wikipedia.org/wiki/Serdes, viewed April 23, 2007). A search of http://www.google.com for SERDES results in about 482,000 references. In addition, the present application is replete with exemplary implementations and information regarding various aspects of SERDES.

Applicant respectfully asserts that the scope of the claimed subject matter, including what is meant by SERDES, can easily be determined by one having ordinary skill in the art, and the rejection is therefore not appropriate. "If the scope of the claimed subject matter can be determined by one having ordinary skill in the art, a rejection using this [35 USC § 112] form paragraph would not be appropriate." (MPEP 7.34.01 Examiner Note 2.) Reconsideration and withdrawal of the 35 USC § 112 rejection of claims 1, 11, 12, 21, and 24 is respectfully requested.

In addition, the examiner alleges that claim 12 seems not to have the structure of a system claim. Claim 12 has been amended to present the structure more explicitly. Reconsideration and withdrawal of the 35 USC § 112 rejection of claim 12 is respectfully requested.

Claim Rejections - 35 USC § 103

Claims 1-24 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over Benson (U.S. Pat. No. 5,907,566, hereinafter "*Benson*") in view of Chandran (U.S. Pat,. No. 5,068,854, hereinafter "*Chandran*"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case for obviousness under 35 USC § 103(a), it must be shown that the asserted references, when read alone or in combination, teach all of the elements of the examined claims. Also, a motivation to combine the references may be shown if more than one reference is being asserted, *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, slip opinion 04-1350 page 15 (April 30, 2007).

Furthermore, the factual inquiries set forth in *Graham v. John Deere*, 383 U.S. 1 (1966), should be applied to establish a background for determining obviousness under 35 USC § 103(a). Those inquiries are: determining the scope and contents of the prior art; ascertaining the differences between the prior art and the claims at issue; resolving the level of ordinary skill in the pertinent art; and considering objective evidence present in the application indicating obviousness or non-obviousness.

The claimed invention pertains to a data communications architecture employing serializers and deserializers communicating over links (so-called SERDES links) for use in communicating data between computer processing components of a computing environment. In disclosed exemplary implementations and in the claims, "one or more operatively coupled

SERDES communication links" provide for high speed, low latency communications, such as for use in a computer infrastructure (see, e.g., paragraph **[0026]**, "the illustrative implementation may orchestrate the use of multiple parallel SERDES communications channels"; Figs. 2-4 showing transmit and receive cores each having one or more operatively coupled SERDES communication links whose operation is orchestrated by logic blocks). The phrase "one or more operatively coupled SERDES communication links" necessarily comprises more than a single link because a single link can not be "operatively coupled" to itself. As shown in Figs. 2-4 and described in paragraphs [0036]-[0038], each of the physical links 220 comprises a SERDES communication path. The dashed box 215 shows the components of an exemplary data communications backplane. In the exemplary backplane, a plurality of SERDES links communicate data from transmit core 235 to receive core 245, illustratively shown disposed on data interface cards 205 and 210, respectively; and a plurality of SERDES links also communicate data from transmit core 250 to receive core 240. As disclosed in paragraph [0037], "data may be communicated in a selected direction or bi-directionally, as indicated by the arrows on physical links 220 and data 230, between transmit cores and receiving cores of data communications interfaces 205 and 210." Paragraph [0038] discloses that "transmit-receiving core pairs 235, 240 and 245, 250 may cooperate to form a communications channel." Figs. 3 and 4 show exemplary transmit and receive cores, respectively. Each transmit and receive core comprises a plurality of serializers and deserializers, respectively. In the exemplary implementation, the operation of the serializers and deserializers is orchestrated by logic blocks in the transmit and receive cores, respectively, to provide the operatively coupled SERDES communication links found in the claims.

In contrast, *Benson* discloses a system for matching off-the-shelf serializing and deserializing circuits that operate at one speed (such as circuits available from the manufacturer AMCC of San Diego, column 2 lines 4-26), with off-the-shelf asynchronous transfer mode (ATM) interface chip sets (such as the Atlanta chip set ATM interface by Lucent Technologies, column 2 lines 28-41). One object of *Benson* is "to use encoding/decoding and serialization/deserialization circuitry developed for other applications to reduce costs," (column 2 lines 48-51). As disclosed in *Benson* column 3 lines 3-25 and column 4 lines 25-45, the chip set processing the ATM word stream (e.g., the Atlanta chip set) operates at 100MHz, while the SERDES chip set (e.g., from AMCC) operates at 125 MHz. *Benson* introduces "a frequency increasing encoder to receive the continuous stream of ATM data cells, and increase the frequency to allow adding additional control words ... The frequency increasing encoder combines the original data words, with additional control words to form a combined word stream at a frequency higher than the frequency of the word stream from the ATM interface and at an available frequency for the ... SERDES chips." (Column 3 lines 3-25.) A frequency decreasing decoder is used to perform the reverse operation at the receiving end (column 4 lines 6-24).

The examiner contends that *Benson* discloses a system to detect errant data communicated across a data communications architecture comprising one or more operatively coupled SERDES communication links, citing Fig. 2 and column 6 lines 13-31. However, *Benson* does not disclose a data communications architecture comprising operatively coupled SERDES communication links, at the cited location or elsewhere. Instead, *Benson* discloses only a single serial data stream communicated over a single SERDES communication path, for example, "in the serializer 11, the combined word stream 9, which was parallel, is converted into a serial data stream and is transmitted over a serial data path 13," (column 5 lines 59-62,

referring to Fig. 2). Because *Benson* does not disclose a plurality of serial data streams communicated using operatively coupled serializers, deserializers, or SERDES communication paths, as disclosed in the present application, *Benson* cannot be used to detect errant data in anything like the manner of the claimed invention.

In addition, *Chandran* also does not disclose or suggest the features of operatively coupled serializers, operatively coupled deserializers, and/or operatively coupled SERDES communication links. *Chandran* teaches error detection of digital data transmitted on a single optic link, without generating a large amount of overhead or degrading bandwidth. A check code is generated for data to be sent. The data is sent serially over the optical link, followed by the check code. At the receiving end, an error code is developed from the information packet in the same manner as the check code. The error code (from the transmitting end) and the check code (from the receiving end) are then compared to one another. If a mismatch is detected, an error signal is generated, indicating that an error may have occurred during transmission. (Column 2 lines 12-24). Like *Benson*, *Chandran* does not teach or suggest a data communications architecture comprising operatively coupled SERDES communication links, or error detection for use in such an architecture.

Thus, neither *Benson* nor *Chandran*, either alone or in any possible combination, teach or suggest the feature of operatively coupled SERDES communication links. Because this feature is found in all claims, the examiner cannot make out a *prima facie* case of obviousness under 35 USC § 103(a).

Although the office action rejects all of claims 1-24 under 35 U.S.C. § 103(a) as being allegedly unpatentable over *Benson* in view of *Chandran*, the action does not attempt to support

the rejection as to claims 1-11. Nevertheless, based on the arguments presented above, if such a rejection of claims 1-11 were to be made, it also cannot be supported.

Claims 1-11 and 24 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over Fredrickson (U.S. Pat. No. 6,154,870, hereinafter "*Fredrickson*") in view of *Benson* (same as above). Applicant believes the examiner meant this 103 rejection to refer to Ramamurthy *et al.* (U.S. Pat. No. 5,790,563, hereinafter "*Ramamurthy*") instead of *Benson*, because the § 103(a) arguments refer to *Ramamurthy* and not *Benson*. With this understanding, applicant respectfully traverses this rejection.

Applicant respectfully notes that neither *Fredrickson* nor *Ramamurthy*, either alone or in any possible combination, teach or suggest the feature of operatively coupled SERDES communication links. Because this feature is found in all claims, the examiner cannot make out a *prima facie* case of obviousness under 35 USC § 103(a).

In addition, with regard to all of the obviousness rejections under 35 USC 103(a), applicant respectfully points out that there is no teaching or suggestion in any of the cited references to combine their features, nor is there any standard practice in the art that would lead one of ordinary skill to combine their features. Therefore, it is respectfully submitted that it is only with impermissible hindsight that the examiner has combined the cited references.

Applicant further observes that this 35 USC § 103(a) rejection of claims 1-11 and 24 appears to be identical to the same rejection found in the previous office action. The Examiner states in paragraph 6 of the most recent action that applicant's arguments with respect to all of claims 1-24 have been considered but are moot in view of new grounds of rejection. However, no new grounds have been presented with regard to claims 1-12 and 24. Applicant has already

traversed and argued against this rejection in the previous office action. Applicant respectfully requests that the examiner reconsider and respond to the applicant's previously presented arguments, repeated here for the examiner's convenience.

Fredrickson discloses a new Viterbi Partial Response Maximum Likelihood (PRML) error-correction protocol and system. A signal sequence of 8-bit bytes is fed to an encoder that produces 9-bit sequences. These signals are fed to a serializer to produce a precoder input signal, which is fed into a precoder. The precoder outputs a sequence that is transmitted over a medium that is subject to signal degradation caused by noise contamination. A receiver recovers the possibly noisy signal, and feeds it to a Viterbi detector. The detector forms an estimate of the precoder output signal, which is input to an inverse precoder function to yield an estimate of the precoder input signal. This is fed to a deserializer and deserialized into 9-bit subsequences, which are fed to a decoder to produce an estimate of 8-bit data bytes, as reconstructed to be freed from noise corruption. The resulting output signal is representative of the original signal sequence of 8-bit bytes, despite the imposition of noise corruption during transmission. This arrangement is described to be an example of so-called forward error correction, which allows the receiver to detect and correct errors without the need to ask the sender for additional data. Thus, unlike the present application, no provision is made in *Fredrickson* for retransmission of errant data.

The Examiner asserts that *Fredrickson* calculates a disparity for data being communicated, calculating an error code based on the calculated disparity (citing *Fredrickson* col. 4 line 40 to col. 5 line 3), communicating data between a serializer and a deserializer then calculating a disparity on the received data to generated another error code (citing *Fredrickson* col. 3 lines 3-12). However, these features are not found at the cited locations, nor elsewhere in

Fredrickson. *Fredrickson* col. 3 lines 3-12 appears to be discussing known usages of so-called convolutional codes, a type of error-correction wherein each m-bit information symbol (here, m=8) is transformed into an n-bit symbol (here, n=9), where m/n is the code rate (here, 8/9), and the transformation is a function of a certain number of adjacent symbols. Such codes have nothing at all to do with the present application.

Fredrickson col. 4 line 40 to col. 5 line 3 describes the generation of these convolutional codes. The code generation of *Fredrickson* does not teach the present application's calculating a disparity for data being communicated by one or more operatively coupled serializers, nor calculating an error code based on the disparity, nor calculating a disparity on the received data to generate another error code, as recited in independent claims 1, 11, and 24 of the present application.

Because the Examiner relies on *Fredrickson* to teach the limitations of the present application in all 35 USC § 103 rejections, the rejections do not support a *prima facie* case of obviousness under 35 USC § 103(a). Withdrawal of the 35 USC § 103 rejection of claims 1-11 and 24 is respectfully requested.

Conclusion

In view of the foregoing amendment and remarks, Applicant respectfully submits that the present application, including claims 1-24, is in condition for allowance and an early notice of allowance is respectfully requested.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help

to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Respectfully submitted,

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